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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/675,721 | 09/30/2003 | Frank Eliot Levine | AUS920030483US1 | 6347 |

35525 7590 04/09/2008

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

| EXAMINER | |
|---|---|
| VO, TED T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2191 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 04/09/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptonotifs@yeeiplaw.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/675,721 | LEVINE ET AL. | |
| | Examiner | Art Unit | |
| | TED T. VO | 2191 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *26 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,9,10,17,18 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9,10,17,18 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

1. This action is in response to the communication filed on 12/26/2007.

Claims 1-2, 9-10, 17-18, 25 are pending in the application.

***Response to Arguments***

2. Response to Applicants' arguments:

- With regard to the rejection of Claims 17-18 under 35 USC 101, Applicants have amended the medium as "a computer recordable medium". This medium is direct to the specification: "Examples of computer readable media include recordable-type media, such as a floppy disk, a hard disk drive, a RAM, CD-ROMs, DVD-ROMs".

Therefore, the medium in the claims is direct to the type addressed in the specification. The rejection of these claims in view of the amendment is withdrawn.

- With regard to the rejection of Claims 1-2, 9-10, and 17-18 under 35 USC 112, second paragraph, Applicants have not directly explained "indicator", but merely point the slots of Figure 5, which contains instruction bits of execution units. Thus, the indicators as referred by the argument are as instructions brought to a performance monitor unit in profiling. The rejection of claims 1-2, and 9-10, and 17-18 is without in view of the argument. The "indicators" will direct to a set of instructions that are carried out in profiling.

- With regard to the rejection of Claims 1-2, 9-10, and 17-18 under Intel, it appears the argument is that Intel fails to teach the features of "identifying a routine that is used more than a threshold number of times during execution of the program as a routine of interest," and "responsive to identifying the routine of interest during execution of the program, dynamically associating instructions in the identified routine of interest with a set of performance indicators to form a modified routine, wherein the set of performance indicators comprises one of a set of performance indicators comprising one or more bits located in fields within the instructions and a set of performance indicators comprising metadata located in a shadow memory, and wherein the set of performance indicators identify that the instructions are to be monitored.". The remarks argued that Intel does not teach a set of performance indicators as recited in claim 1.

Examiner disagrees: The teachings of Intel are mapped as provided in this action. Intel performance monitor set many counters. For example, see sec. 6.1.2: "performance monitor counts have to be associated with program locations", and see the monitoring events, they are the events such as cache miss, branch misprediction, etc. The information in the description of Intel profiling directs to the recitation "identifying routine", and "performance indicators". According to the Applicants' specification, it directs the "performance indicators" as the slots of instructions carried out under the performance monitor. The Intel thus does the same.

-Applicants' remarks further argued that Intel fails to teach the feature of "identifying a routine that is used more than a threshold number of times during execution of the program as a routine of interest".

Examiner disagrees: In the specification, "threshold number of times during execution", merely direct to the number of processors or clock cycles for instruction execution that may pass

before events should be counted. As seen in the reference, the profiling monitor of Intel does the same.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 9-10, 17-18, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Intel, "Intel IA-64 Architecture Software Developer's Manual", Revision 1.1, Vol. 4, No. 245320-002, 7-2001.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1: Intel reference has 8 sections. Intel discloses,

***A method in a data processing system for monitoring execution of instructions, the method comprising: executing a program*** (See Figure 6-2 in p. 4 of sec. 6);

***Identifying a routine that is used more than a threshold number of times*** (See sec. 6.1.2 "profiling", refer to "performance monitor counts have to be associated with program locations

(*'identifying a routine'*)". Further more see sec. 6.1.1.2, 6.1.1.3 (p.6-3), sec. 6, p. 6, see event counter; The profiling' counter events are calculating based on times) ***during execution of the program as a routine of interest*** (See sec. 6.1.1.3, particularly, see its second paragraph. Intel discloses an identifying of a routine such as a benchmark is tested with different threshold values for identifying the performance "knee");

***responsive to identifying the routine of interest during execution of the program, dynamically associating instructions in the identified routine of interest with a set of performance indicators*** (sec. 6, p.7, i.e. triggers on events shown in table 6-2, see in the near end of the page, "registers indicate to…", see table 6.3, p. 10-11, and sec. 6, p. 13, "PMC/PMD register assignments for each monitoring feature…") ***to form a modified routine*** (See sec. 6, p. 5, "are interesting identifying performance bottlenecks and relating them back to their source code": *identifying a routine of interest during execution of a program; then see "code instrumentation", in p. 26 of sec 6* **), *wherein the set of performance indicators comprises one of a set of performance indicators comprising one or more bits located in fields within the instructions*** (See Figure 6-5, that detects indicators as instructions instrumented in the IA-64 instruction execution. These instructions are seen in sec. 7, such as instruction PIPELINE_FLUSH. Also see "performance monitor events , event counters, seen in sec. 6.1.2.2, and 6.1.2.3, p. 3, or program counter sampling for identifying hot spot, see in sec. 6, p.6 – Note: See a performance counter "monitor ++" that is implemented in a program shown in sec. 7, p.25, if take performance counters as performance indicators then each of these counter comprising 32-bits) ***and a set of performance indicators comprising metadata located in a shadow memory*** (Each of instructions shown in the sec. 7 is associated with associated with event code, and registers

such as PMC/PMD (See table 6.3, p. 10-11, and sec. 6, p. 13, "PMC/PMD register assignments for each monitoring feature…"- Note if take the performance counter "monitor ++" in the program as shown in sec. 7, p. 25, then the data of this instruction is generated and stored in a shadow of a branch predict_instruction (i.e. *metadata*) (e.g. see sec. 7, p. 33, the definition in INST_ACESS_CYCLE)***, and wherein the set of performance indicators identify that the instructions are to be monitored;*** (For example, monitoring cache; or see sec. 6.2.2 for setting maximum per-cycle event increment, etc); ***and***

***responsive to execution of an instruction in the modified routine*** (i.e. the routine contains hotspot results by profiling) ***during continued execution of the program, incrementing a counter*** (i.e., the performance counters. For example, see sec. 6, Figure 6-5, p. 7), ***wherein the counter provides a value identifying a number of times that the instruction in the modified routine is executed*** (e.g. sec. 6.2.2, p.16 of sec. 6).

As per Claim 2: Intel discloses, ***The method of claim 1 further comprising: associating instructions in a second routine of interest with a second set of indicators to form a second modified routine*** (Intel discloses a program that has many routines, and each of routine in monitored)***; and responsive to execution of an instruction in the second modified routine, incrementing a second counter*** (See sec. 6, Figure 6-5, p. 7).

As per Claims 9-10: See rationale addressed in the rejection of claims 1-2 above.

As per Claims 17-18: See rationale addressed in the rejection of claims 1-2 above.

As per Claim 25: See rationale addressed in the rejection of claims 1-2 above.

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
March 27, 2008

/Ted T. Vo/
Primary Examiner, Art Unit 2191